

### **REMARKS**

Claim 17 has been amended for clarification. Amended claim 17 recites multiplying an original frequency of a second signal by a multiplier value. Amended claim 17 recites adjusting the multiplier value to the corrected multiplier value to produce a desired frequency, and at the frequency source, producing an output signal having an output frequency, which is approximately equal to the desired frequency, by multiplying the original frequency by the corrected multiplier value.

Claim 23 has been amended to add changes similar to those of claim 17.

Claim 27 has been amended for clarification. Amended claim 27 recites multiplying an input frequency of an input signal, and a multiplier having a value. Amended claim 27 recites that the controller adjusts the value of the multiplier based on the measurement data, and the frequency source produces a signal by multiplying the input frequency and the adjusted multiplier value.

The amendment to the claims is fully supported by the application as originally filed. No new matter has been introduced by way of the amendment. Support for the amendment to claims 17, 23 and 27 can be found, for example, on former claims 17, 23 and 27, and on page 6, lines 8 to 29. No new matter has been introduced by way of the amendment. Applicant respectfully requests the Examiner to enter the above amendment.

The Examiner stated that (former) claims 18, 25 and 26 would be allowable if they are written in independent form.

Applicant has added new claims 33 to 35. New claims 33 to 35 are identical to former claims 18, 25 and 26 except formality. Applicant respectfully submits that new claims 33 to 35 are in allowable state.

The Examiner rejected claims 17, 19, 20, 23, 24, 27, 30 and 32 under 35 U.S.C. 102(e) as being anticipated by Sunter et al. (U.S. Patent No. 6,396,889), hereinafter referred to as Sunter. The Examiner rejected claims 21, 22, 28, 29 and 31 under 35 U.S.C. 103(a) as being unpatentable over Sunter.

Claims 17, 23 and 27 are independent claims. Claims 17, 23 and 27 recites a frequency source for multiplying a signal by a multiplier value, and (a controller for) adjusting the multiplier value.

Sunter discloses a phase locked loop (PLL) 10 and its testing circuit. The testing circuit is provided to determine whether the PLL 10 passes or fails the test (col. 5, lines 28 to 32, col. 6, lines 53 to 55, col. 7, lines 27 to 29, and col. 8, lines 4 to 6 of Sunter).

The testing circuit 80 of Figure 5 in Sunter includes a clock source, a controller 32, a multiplexer 34 and a frequency measurement. The clock source provides a reference input 14 to the multiplexer 34. The controller 32 provides a Test Mode signal 40 and a feedback clock signal 42 to the multiplexer 34. The multiplexer 34 has two input node, namely node "1" and node "0".

The Examiner stated: Sunter indeed teaches a multiplexer 34 is a multiplier (see fig. 5, two inputs 14 and 42 into multiplexer 34 and only one output "PLL". Applicant respectfully disagrees with the Examiner for reasons set out below.

Col. 4, lines 39 to 40 of Sunter states "Multiplexer 34 is controlled by a Test Mode signal 40". Col. 4, lines 62 to 65 of Sunter states: "...the controller 32 outputs a logic high Test Mode signal to select the feedback clock input 42 instead of the input clock 14". [Emphasis added]. Col. 6, lines 19 to 22 of Sunter states: "...controller 32 enables the feedback with a 90° phase shift by applying a logic high (step 84) to the control input of multiplexer 34 to select the feedback clock 42 instead of the input clock 14." [Emphasis added]. It is respectfully submits that the multiplexer 34 accepts the reference signal 14 ("0" input) or the feedback clock 42 ("1" input) based on the Test Mode signal 40. The multiplexer 34 does not multiply the reference signal 14 by the feedback clock 42. Accordingly, the controller 32 does not provide a multiplier value to the multiplexer 34, and does not adjust the multiplier value.

Sunter neither discloses nor suggests adjusting the multiplier value to the corrected multiplier value, and at the frequency source, producing an output signal having an output frequency, which is approximately equal to the desired frequency, by multiplying the original frequency by the corrected multiplied value as recited in claim 17.

Sunter neither discloses nor suggests adjusting the multiplier value based on a desired frequency and a measurement of the preliminary frequency to produce the corrected multiplier value, and at the frequency source, outputting a signal having an intermediate frequency by multiplying the original frequency by the corrected multiplied value as recited in claim 23.

Sunter neither discloses nor suggests a combination of a frequency source, a frequency measurement and a controller as recited in claim 27.

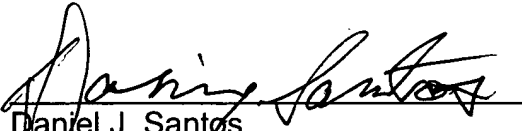
During the test mode, the multiplexer 34 selectively provides one input to the PLL 10, and the controller 32 counts PLL output cycles (col. 6, lines 24 to 27, step 86 of Figure 6, col. 6, lines 28 to 33, and step 94 of Figure 6 of Sunter). Based on the counts, the average change in PLL output frequency is determined (col. 6, lines 49 to 50 of Sunter). It is determined based on the average change whether the PLL passes or fails the test (col. 6, lines 50 to 55, and step 97 of Figure 6 of Sunter). The object of Sunter is to find a PLL condition. Sunter neither addresses calibrating radio by adjusting a multiplier value.

Hence it is respectfully submitted that claims 17 to 32 are patentable in view of the cited reference.

**CONCLUSION**

For the reasons set forth above, it is respectfully submitted that all pending claims are now in condition for allowance, and Applicant requests a Notice of Allowance be issued in this case. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,  
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